

# Genius

## Semiconductor Device Simulator

Version 1.0.0

### Application Notes: Trapping of Carriers

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## Introduction

The carrier capture and emission at bound states within the bandgap of semiconductors is one of the important fundamental processes in semiconductor devices, and have enormous implications to the device performance. For example, Au dopants were intentionally introduced to BJT devices to reduce the carrier lifetime and improve high frequency performance. The surface states at the oxide/silicon interface has always been a critical issue for the performance and reliability of MOSFET devices.

In this chapter, we will demonstrate the simulation of charge trapping related processes in PN diode and MOSFET devices, using the Genius device simulator.

## Carrier Capture and Emission Dynamics

The conduction and valence bands can exchange carriers with a trap in the bandgap in four basic processes, namely electron capture, electron emission, hole capture and hole emission, as depicted in Figure. The concentration of trapped electrons in a trap is governed by the rate equation,

$$\frac{\partial n_T}{\partial t} = C_N - E_N - C_P + E_P \quad (1)$$

where  $n_T$  is the concentration of electrons trapped at the bound state, and  $C_N$ ,  $E_N$ ,  $C_P$  and  $E_P$  represents the rate of electron capture, electron emission, hole capture and hole emission, respectively. The four rates are generally expressed in the following

$$C_N = \sigma_n v_n n (N_{TT} - n_T) \quad (2a)$$

$$E_N = \sigma_n v_n n_T n_i e^{(E_T - E_i)/kT} \quad (2b)$$

$$C_P = \sigma_p v_p p n_T \quad (2c)$$

$$E_P = \sigma_p v_p (N_{TT} - n_T) n_i e^{(E_i - E_T)/kT}. \quad (2d)$$

The concentration of traps is  $N_{TT}$ , while the concentration of captured electrons is  $n_T$ . The capture cross-section of the trap for electrons and holes are  $\sigma_n$  and  $\sigma_p$ , and the respective carrier thermal velocities are  $v_n$  and  $v_p$ . The trap state resides at the energy level  $E_T$  with respect to the intrinsic fermi level  $E_i$ .

## Implementation in GENIUS

In a standard drift-diffusion solver, every node is associated with three state variable, the electrostatic potential  $\psi$ , the electron concentration  $n$ , and hole concentration  $p$ . For each type of traps at this node, one additional state variable is needed for  $n_T$ , the concentration of trapped electrons. Accordingly, the additional equation **Equation (1), p. 1** must be solved for each trap.

There are two common approaches to solve the additional trapping equations. The first is to couple the trap equations with the drift-diffusion equations, which are then solved together. When there are many different traps associated with each trap, this would be numerically inefficient. In the second approach, the trap equations are solved separately, but self-consistently, with the drift-diffusion equations. In GENIUS, the self-consistent approach is chosen, as described below.

The drift-diffusion equations are the solved in the main Newton iterations. In each iteration, the electron and hole concentration ( $n$  and  $p$ ) from the previous iteration are fed to the charge trapping module, which are implemented through the physical model interface (PMI). The trap PMI solves **Equation (1), p. 1** for the concentration of captured electron  $n_T$ . One can calculate the rate of electrons and holes being removed from the conduction and valence bands, respectively, using

$$R_n = C_N - E_N \quad (3a)$$

$$R_p = C_P - E_P \quad (3b)$$

with carrier capture and emission rates calculated from **Equation (2), p. 1**. Since this equation is linear in  $n_T$ , the solution can be treated as exact, apart from the local truncation error (LTE) due to time stepping.

For acceptor traps, the electronic state bears one unit of negative charge when occupied by an electron, and is neutral when empty. For donor traps, on the other hand, the electronic state is neutral when occupied, and bears one unit of positive charge when empty. The trapped charge is thus

$$\rho_T = \begin{cases} -qn_T & \text{for acceptors} \\ q(N_{TT} - n_T) & \text{for donors.} \end{cases} \quad (4)$$

After the  $R_n$ ,  $R_p$  and  $\rho_T$  are obtained, they are feedback to the main DD solver and appear in the continuity equation of electron, hole and the Poisson equation, respectively.

This cycle between the main DD solver and the trapping PMI continues, until the main solver determines that the error residual is below tolerance. The time step in transient simulation is determined by the main DD solver. Since the time constants of the capture/emission processes are typically much longer than that of carriers in

conduction and valence bands, this should not introduce additional error.

Since  $n_T$  is highly nonlinear in  $n$  and  $p$ , the inclusion of the trapping equations occasionally leads to numerical difficulties in the energy balanced solver, when the local carrier densities are lower than the trap density. This situation might occur in the simulation of bipolar devices. To improve stability, one can choose to treat the traps as electrically neutral, which is usually a good approximation in bipolar devices.

## Simulation of PN Diode with Traps

Deep-level defects in PN diodes are known to reduce the carrier lifetime, and cause the diode leakage current to increase. In this section, we describe the procedure of simulating a PN diode that is doped with deep-level traps, with the input file shown below.

Input file to simulate the PN diode with traps

```

1  #=====
2  # GENIUS example: PN Diode simulation with Traps
3  # The usage of Trap PMI is demonstrated here
4  #=====
5
6  # Create an initial simulation mesh
7
8  GLOBAL      T=300 DopingScale=1e18  Z.Width=1.0
9
10 MESH        Type = S_Tri3 #triangle="pzADq30Q"
11
12 X.MESH      WIDTH=1.0  N.SPACES=5
13 X.MESH      WIDTH=1.0  N.SPACES=5
14 X.MESH      WIDTH=1.0  N.SPACES=5
15
16 Y.MESH      DEPTH=1.0  N.SPACES=5
17 Y.MESH      DEPTH=1.0  N.SPACES=5
18 Y.MESH      DEPTH=1.0  N.SPACES=5
19
20
21 # Specify silicon and electrode regions
22 REGION      Label=Silicon  Material=Si
23 REGION      Label=Cathode  Material=Elec Y.min=2.8 Y.max=3.0
24
25 FACE        Label=Anode    Location=TOP    x.min=0 x.max=1.0
26
27 DOPING      Type=Analytic
28 PROFILE     Type=Uniform    Ion=Donor      N.PEAK=1E15  \
29             X.MIN=0.0 X.MAX=3.0 Y.min=0.0 Y.max=3.0
30 PROFILE     Type=Analytic   Ion=Acceptor   N.PEAK=1E19  \
31             X.MIN=0.0 X.MAX=1.0 X.CHAR=0.2  \
32             Y.min=0.0 Y.max=0.0 Y.JUNCTION=0.5
33
34 # Concentration of traps
35 PROFILE     Type=Uniform    Ion=Custom    ID=TrapA N.Peak=1e15  \

```

## Simulation of PN Diode with Traps

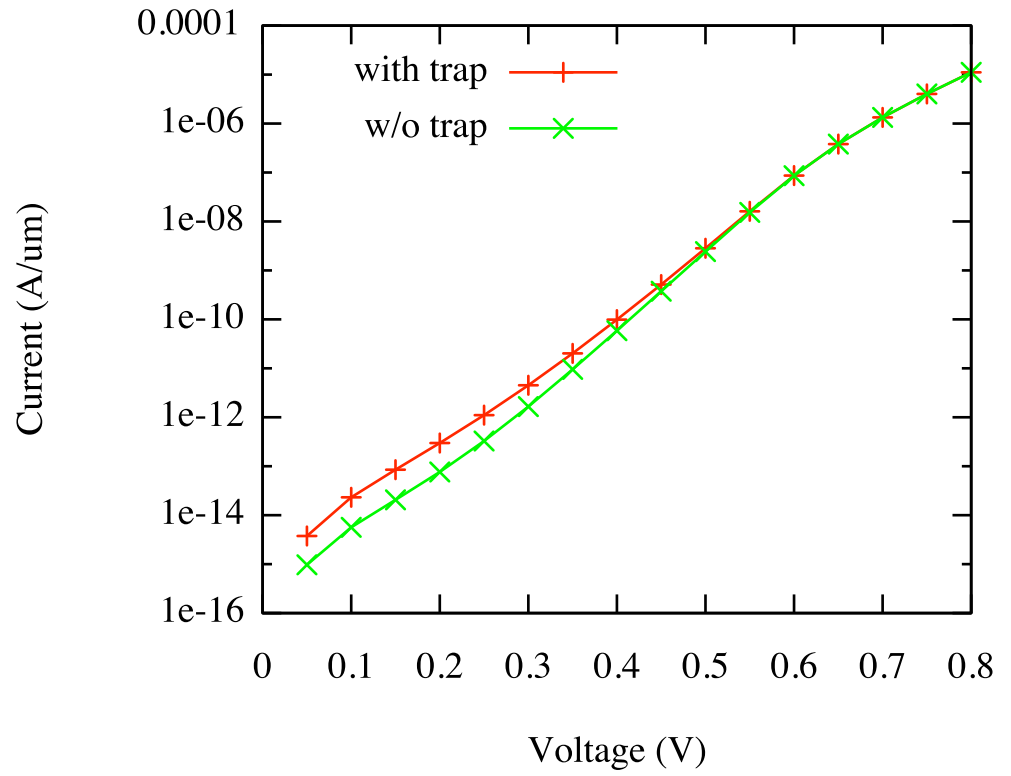
```
36         X.min=0.0 x.max=3.0 Y.min=0.0 Y.max=1.0
37
38 # Boundary conditions
39 BOUNDARY ID=Anode Type=Ohmic
40 CONTACT ID=Cathode Type=Ohmic
41
42 # Refine the mesh
43 REFINE.C Variable=Doping error.fraction=0.7 Measure=signedlog
44 METHOD Type=Poisson NS=Basic
45 SOLVE
46
47 REFINE.C Variable=Potential error.fraction=0.7
48 METHOD Type=Poisson NS=Basic
49 SOLVE
50
51 REFINE.C Variable=Potential cell.fraction=0.4
52 METHOD Type=Poisson NS=Basic
53 SOLVE
54
55 # Setup the traps
56 PMI Region=Silicon Type=Trap string<Profile>="TrapA" \
57     string<ChargeType>=Acceptor double<Prefactor>=1.0 \
58     double<Energy>=0.02 double<sigman>=1e-16 double<sigmap>=1e-14
59 PMI Region=Silicon Type=Trap string<Profile>="TrapA" \
60     string<ChargeType>=Donor double<Prefactor>=1.0 \
61     double<Energy>=-0.22 double<sigman>=5e-15 double<sigmap>=2e-15
62
63 # Solve for the I-V curve
64 MODEL Region=Silicon Mobility.Force=EQF Trap=true
65 METHOD Type=DDML1 NS=Basic LS=BCGS
66 SOLVE TType=EQ
67 SOLVE TType=DCSWEEP Vscan=Anode Vstart=0.0 Vstep=0.05 \
68     Vstop=0.8 out.prefix=diode_iv
```

In lines 1-32, we setup the mesh and doping profile of the PN diode as usual.

In lines 34-36, we define the concentration of traps in the device. Most importantly, we loads the trap PMI in lines 55-61 and define two types of traps, whose concentrations are associated with the profile *TrapA* and scaled with Prefactor. The ChargeType can be Acceptor, Donor or Neutral. The energy level of the trap with reference to the intrinsic Fermi level is set with the parameter Energy, and the capture cross-sections with sigman and sigmap. One may notice that the trap parameters corresponds to gold ions in silicon.

From line 63 and on, we solve for the IV curves in the forward-biased diode, and the result is plotted in **Figure 1, p. 6**. It is observed that, with traps included, the

leakage current at low bias increases significantly.



**Figure 1** IV curves of the forward-biased diode with traps.

## Simulation of MOSFET with Interface Traps

In this section we turn to the simulation of interface traps in MOSFET. Interface traps lead to degradation in the sub-threshold swing, and shift in the threshold voltage. High level of interface traps also cause degradation in carrier mobility. The study of interface traps has been a continuing theme throughout the development of MOS technology. The simulation procedure of MOSFET with interface traps is demonstrated in this section. We first generate the MOSFET mesh structure.

Input file to generate MOS structure for interface trap simulation.

```

1  #=====
2  # GENIUS Example. Build NMOS with Triangle mesh
3  #=====
4
5  GLOBAL      T=300 DopingScale=1e18 Z.Width=1.0
6
7  # Create an initial simulation mesh
8  MESH        Type = S_Tri3 Triangle="pzAQ"
9
10 X.MESH      X.min=-0.29 WIDTH=0.20  N.SPACES=20
11 X.MESH      WIDTH=0.18  N.SPACES=36
12 X.MESH      WIDTH=0.20  N.SPACES=20
13
14 Y.MESH      Y.TOP=-0.0037 DEPTH=0.0037 N.SPACES=4
15 Y.MESH      DEPTH=0.1  h1=0.005 h2=0.01
16 Y.MESH      DEPTH=0.4  h1=0.01 h2=0.05
17
18 # Eliminate some unnecessary substrate nodes
19 ELIMINATE Direction=Y X.min=-0.29 X.max=0.29 Y.TOP=0.3
20
21 # Specify oxide and silicon regions
22 REGION      Label=NSilicon  Material=Si
23 REGION      Label=NOxide    IY.MAX=4 Material=0x
24 REGION      Label=NSource   X.min=-0.29 X.MAX=-0.19 IY.MAX=4 Material=Elec
25 REGION      Label=NDrain    X.max=+0.29 X.MIN=+0.19 IY.MAX=4 Material=Elec
26
27 # Specify interfaces
28 FACE        Label=GIF IY=4 x.min=-0.09 x.max=0.09 Direction=YNorm
29 FACE        Label=SUB Location=BOTTOM
30 FACE        Label=GATE Location=Top X.MIN=-0.09 X.MAX=0.09
31
32 # Doping profiles
33 DOPING      Type=analytic

```

```

1  PROFILE  Type=Uniform  Ion=Acceptor  N.PEAK=3E17  X.min=-0.29  X.max=0.29  \
2          Y.min=0  Y.max=1
3  PROFILE  Type=Analytic  Ion=Acceptor  N.PEAK=1E18  X.min=-0.29  X.max=0.29  \
4          Y.min=0.08  Y.max=0.2  Y.CHAR=0.1
5
6  PROFILE  Type=Analytic  Ion=Donor  N.Peak=4E19  Y.Junction=0.05  \
7          X.min=-0.29  X.max=-0.09  XY.Ratio=0.75
8  PROFILE  Type=Analytic  Ion=Donor  N.Peak=4E19  Y.Junction=0.05  \
9          X.max=+0.29  X.min=+0.09  XY.Ratio=0.75
10 PROFILE  Type=Analytic  Ion=Donor  N.Peak=2E20  Y.Junction=0.12  \
11         X.min=-0.29  X.max=-0.18  XY.RATIO=0.75
12 PROFILE  Type=Analytic  Ion=Donor  N.Peak=2E20  Y.Junction=0.12  \
13         X.max=+0.29  X.min=+0.18  XY.RATIO=0.75
14
15 # Boundaries
16 BOUNDARY  ID=SUB  Type=Ohmic
17 BOUNDARY  ID=GATE  Type=Gate  Work=4.17
18 BOUNDARY  ID=GIF  Type=InsulatorInterface
19
20 METHOD     Type=Poisson
21 SOLVE
22
23 EXPORT    VTKFILE=nmos_tri.vtk  CGNSFILE=nmos_tri.cgns

```

The entire interface between the *NOxide* region and the *NSilicon* region is automatically named *NOxide\_to\_NSilicon*. However, we are concerned with the interface traps below the gate only. Therefore, in line 28, we label the interface between gate oxide and the silicon channel as *GIF*. In line 51, it is defined as a insulator/semiconductor interface. The generated structure is saved in *nmos\_tri.cgns*.

Following that, we load in the *cgns* file and simulate the  $I_d$ - $V_g$  characteristics. In lines 20-22, acceptor-like interface traps are created at the *GIF* interface. Note that one should explicitly indicate the Type of the trap to be *Interface*. The surface density is  $N_{it} = 3 \times 10^{11} \text{ cm}^{-2}$ , and the energy level is 0.2 eV above the intrinsic Fermi level.

The simulation results are shown in **Figure 2, p. 10**. It is seen that with one type of interface traps at a single energy level, the sub-threshold  $I_d$ - $V_g$  curve has a kink at  $V_g = 0.3 \text{ V}$ , and the threshold voltage increases.

Input file to simulate the  $I_d$ - $V_g$  curve of MOSFET with interface traps.

```

1  #=====
2  # GENIUS Example. Do IV Scan at Vdrain=0.1V
3  #=====
4

```

## Simulation of MOSFET with Interface Traps

```

5 GLOBAL T=300 DopingScale=1e18 Z.Width=1.0
6
7
8 # voltage sources are needed here.
9 Vsource Type = VDC ID = VDS Tdelay=0 Vconst=0.1
10
11 # Load mesh
12 IMPORT cgnsfile=nmos_tri.cgns
13
14 BOUNDARY ID=SUB Type=Ohmic
15 BOUNDARY ID=GATE Type=Gate Work=4.17
16 CONTACT Type = OhmicContact ID = NSource Res=0 Cap=0 Ind=0
17 CONTACT Type = OhmicContact ID = NDrain Res=0 Cap=0 Ind=0
18
19 # Load Trap PMIS, Specify interface trap
20 PMI Region=NSilicon Type=Trap string<Type>=Interface \
21 string<Interface>=GIF string<ChargeType>=Acceptor \
22 double<IF.Density>=1e11 double<Energy>=0.2
23
24 Model Region=NSilicon H.Mob=false Trap=true
25 METHOD Type=DDML1 NS=Basic LS=BCGS maxiteration=40 Damping=Potential
26 SOLVE Type=STEADY
27
28 PMI Region=NSilicon Type=Mobility Model=Lucent
29 Model Region=NSilicon H.Mob=true Mob.force=EQF Trap=true
30
31 METHOD Type=DDML1 NS=Basic LS=BCGS maxiteration=20 Damping=Potential
32
33 # Ramp up drain voltage
34 SOLVE Type=DC Vscan=NDrain Vstart=0.0 Vstep=0.02 Vstop=0.1
35
36 # Scan gate voltage
37 ATTACH Electrode=NDrain Type=Voltage VApp=VDS
38 SOLVE Type=DC Vscan=GATE Vstart=0.0 Vstep=0.05 Vstop=1.5 out.prefix=gate_iv
39
40 EXPORT VTKFILE=nmos_iv.vtk

```

If interface traps are assigned at a range of different energies in the bandgap, one would expect multiple kinks to occur, and probably blend if the temperature is not too low. This would appear as a change in the sub-threshold slope in the  $I_d$ - $V_g$  characteristics. If we keep the total interface trap density at  $10^{11}$ , but distribute it evenly at three energy levels (0.2 eV, 0.3 eV and 0.4 eV), the resulted  $I_d$ - $V_g$  curve is shown in **Figure 3, p. 11**.

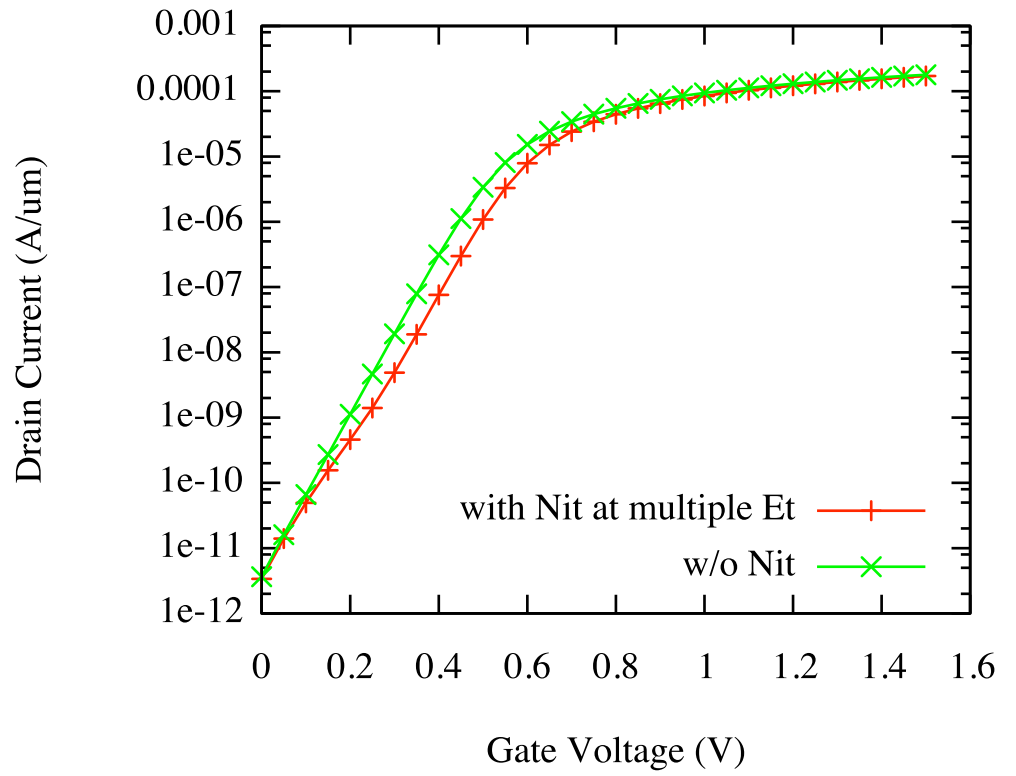
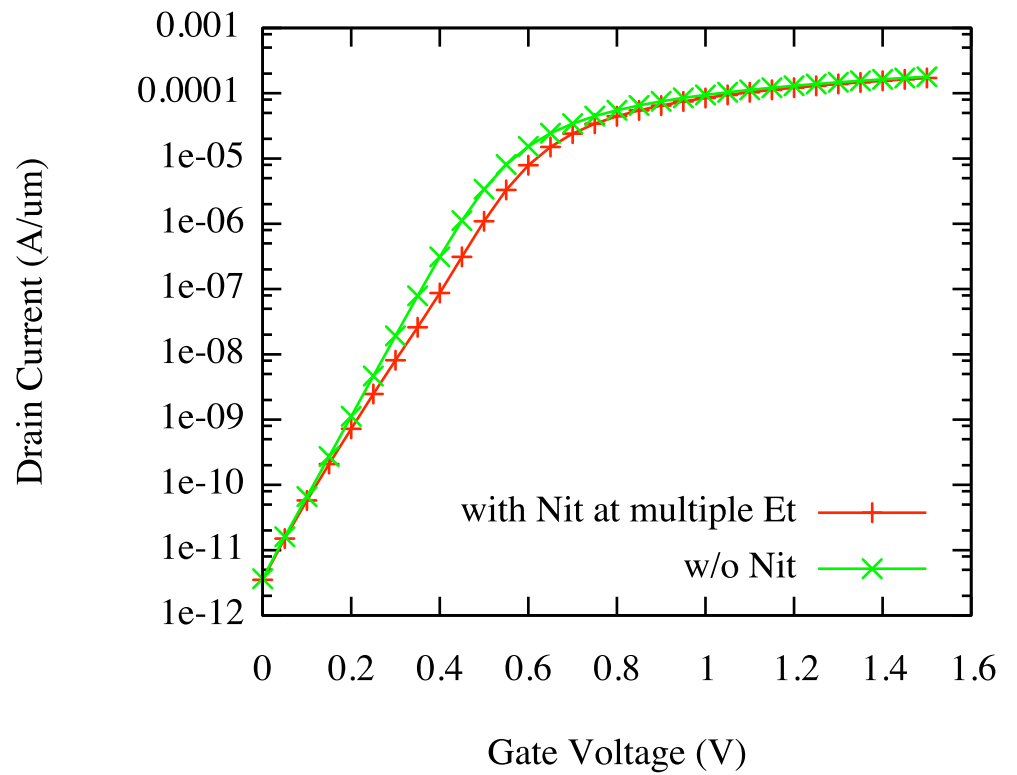


Figure 2 Simulated  $I_d$ - $V_g$  characteristics of the MOSFET with the presence of interface traps.

Simulation of MOSFET with Interface Traps



**Figure 3** Simulated  $I_d$ - $V_g$  characteristics of the MOSFET with multiple interface traps.

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## Summary

In the proceeding sections, we have demonstrated the simulation of traps in semiconductor and semiconductor/insulator interfaces. The effect of deep-level defects in bipolar devices and interface traps in MOSFETs are successfully modelled with the GENIUS devices simulator.