# Genius

## Semiconductor Device Simulator

Version 1.0.0

## Application Notes:
## 3-Dimensional CMOS Inverter

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# Introduction

With the continuous scaling of CMOS technology, the interaction between manufacturing processes and the device characteristics has increasingly become relevant to circuit designers, especially in the design of logic cell library. TCAD engineers are now called upon to simulate small logic circuit cells, preferably in 3-dimensional models.

There are a few alternative ways to simulate small logic circuit cells with TCAD tools. One "traditional" approach is circuit/device mixed simulation, in which one simulates each transistor in TCAD individually and use SPICE to connect the numerical devices. GENIUS is capable of this type of mixed-mode simulation. However, since device simulations are decoupled, the device simulation has to be repeated a few times until the circuit simulator finds the right node voltages for the entire circuit. As a result, mixed-mode simulations are significantly slower.

GENIUS offers an alternative method, in which the circuit cell is simulated as a whole in one TCAD model. We will go through the simulation steps, using a simple CMOS inverter as example in the following sections.

# Mesh Generation and Refinement

The construction of 3D models of circuit cells is non-trivial. GENIUS comes with a utitility EasyCMOS that constructs 3D CMOS meshes from user-supplied mask layout. The generated mesh structure of a simple CMOS inverter is shown in Figure 1, p. 2. This mesh is certanly too coarse to be used in simulation. Therefore, we shall first refine the mesh at critical locations.

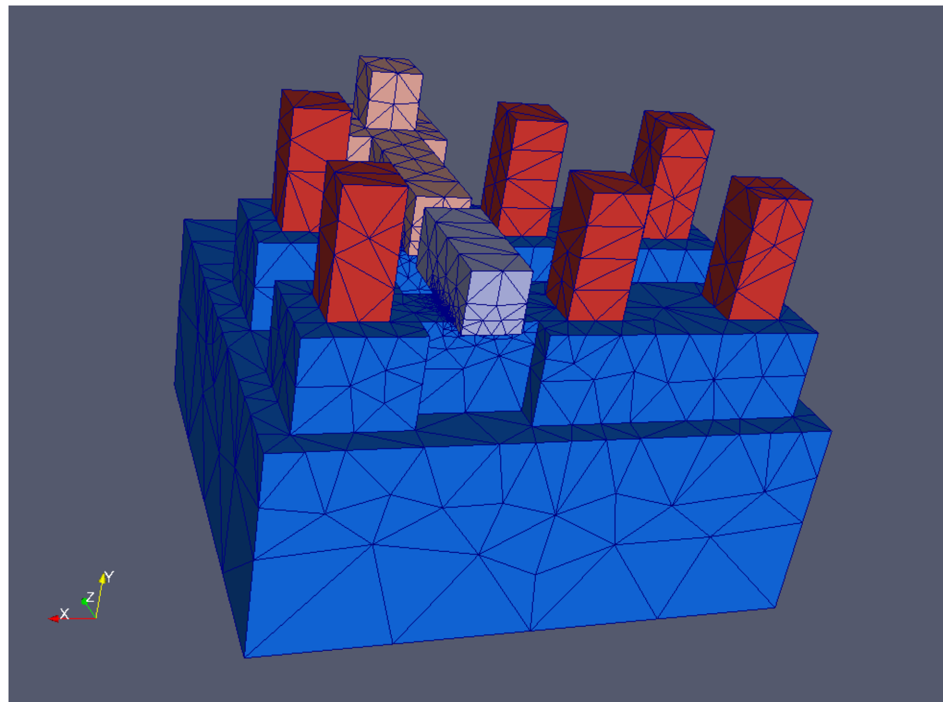


**Figure 1** The input mesh of the CMOS inverter, with the oxide region stripped off.

The EasyCMOS utility creates three files that describes the mesh `inverter.1.node`, `inverter.1.ele` and `inverter.1.face`, along with a skeleton GENIUS input file `inverter.inp` that loads in the mesh files and define the doping profiles. We modify the skeleton file and add a few instructions for mesh refinement.

Input file to define the CMOS inverter and refine the mesh.

```
1  #==============================================================================
2  # Create an initial simulation mesh
3  #==============================================================================
4
5  GLOBAL    T=300 DopingScale=1e18
6
7  MESH      Type = S_Tet4 file.prefix="inverter.1" Tetgen="pzAqV"
8
```

```
9   double    ld=0.09;
10  double    Lsp=0.05;
11
12  # Specify oxide, silicon and electrode regions
13  REGION    Label=Silicon  Material=Si   number=1
14  REGION    Label=NGate    Material=Elec number=2
15  REGION    Label=PGate    Material=Elec number=3
16  REGION    Label=NSource   Material=Elec number=4
17  REGION    Label=PSource   Material=Elec number=5
18  REGION    Label=NDrain    Material=Elec number=6
19  REGION    Label=PDrain    Material=Elec number=7
20  REGION    Label=NWell    Material=Elec number=8
21  REGION    Label=PWell    Material=Elec number=9
22  REGION    Label=Oxide    Material=Ox   number=10
23
24  # And the substrate surface
25  FACE      Label=Sub number=1
26
27  CONTACT   ID=NGate Type=Gate Workfunction=4.17
28  CONTACT   ID=PGate Type=Gate Workfunction=5.10
29  BOUNDARY  ID=Sub   Type=Neumann
30
31  DOPING Type=Analytic
32  # Substrate doping
33  PROFILE   Type=Uniform    Ion=Acceptor N.PEAK=1E16  X.MIN=-100 X.MAX=100  \
34            Z.MIN=-100 Z.MAX=100   Y.min=0.0 Y.max=10
35  # NWell for PMOS
36  PROFILE   Type=Analytic   Ion=Donor    N.PEAK=5e16  X.MIN=-13*ld X.MAX=7*ld \
37            Z.MIN=7*ld Z.MAX=13*ld Y.min=0.15  Y.max=0.25 Y.char=0.2
38  # NMOS channel doping
39  PROFILE   Type=Analytic   Ion=Acceptor N.PEAK=1E18  \
40            X.MIN=-13*ld X.MAX=7*ld Z.MIN=0 Z.MAX=6*ld \
41            Y.min=0.05 Y.max=0.09 Y.char=0.04
42  # PMOS channel doping
43  PROFILE   Type=Analytic   Ion=Donor    N.PEAK=1E18  \
44            X.MIN=-13*ld X.MAX=7*ld Z.MIN=7*ld Z.MAX=13*ld \
45            Y.min=0.05 Y.max=0.09 Y.char=0.04
46
47  # S/D for NMOS
48  PROFILE   Type=Analytic   Ion=Donor    Dose=1e14   \
49            X.MIN=-6*ld  X.MAX=-ld     Z.MIN=0 Z.MAX=6*ld \
50            Y.min=0.00 Y.max=0.012 Y.char=0.012
51  PROFILE   Type=Analytic   Ion=Donor    N.PEAK=1E20 \
52            X.MIN=-6*ld  X.MAX=-ld-Lsp Z.MIN=0 Z.MAX=6*ld \
53            Y.min=0.00 Y.max=0.04 Y.char=0.03
54  PROFILE   Type=Analytic   Ion=Donor    Dose=1E14   \
```

```
55             X.MIN=ld      X.MAX=7*ld     Z.MIN=0 Z.MAX=6*ld \
56             Y.min=0.00 Y.max=0.012 Y.char=0.012
57   PROFILE   Type=Analytic   Ion=Donor     N.PEAK=1E20 \
58             X.MIN=ld+Lsp X.MAX=7*ld     Z.MIN=0 Z.MAX=6*ld \
59             Y.min=0.00 Y.max=0.04 Y.char=0.03
60   # NWell contact
61   PROFILE   Type=Analytic   Ion=Donor     N.PEAK=1E20 \
62             X.MIN=-12*ld X.MAX=-8*ld Z.MIN=7*ld Z.MAX=13*ld \
63             Y.min=0.00 Y.max=0.04 Y.char=0.03
64
65   # S/D for PMOS
66   PROFILE   Type=Analytic   Ion=Acceptor Dose=1e14    \
67             X.MIN=-6*ld  X.MAX=-ld      Z.MIN=7*ld Z.MAX=13*ld \
68             Y.min=0.00 Y.max=0.012 Y.char=0.012
69   PROFILE   Type=Analytic   Ion=Acceptor N.PEAK=1E20 \
70             X.MIN=-6*ld  X.MAX=-ld-Lsp Z.MIN=7*ld Z.MAX=13*ld \
71             Y.min=0.00 Y.max=0.04 Y.char=0.03
72   PROFILE   Type=Analytic   Ion=Acceptor Dose=1e14    \
73             X.MIN=ld      X.MAX=7*ld     Z.MIN=7*ld Z.MAX=13*ld \
74             Y.min=0.00 Y.max=0.012 Y.char=0.012
75   PROFILE   Type=Analytic   Ion=Acceptor N.PEAK=1E20 \
76             X.MIN=ld+Lsp X.MAX=7*ld     Z.MIN=7*ld Z.MAX=13*ld \
77             Y.min=0.00 Y.max=0.04 Y.char=0.03
78   # PWell contact
79   PROFILE   Type=Analytic   Ion=Acceptor N.PEAK=1E20 \
80             X.MIN=-12*ld X.MAX=-8*ld Z.MIN=0 Z.MAX=6*ld \
81             Y.min=0.00 Y.max=0.04 Y.char=0.03
82
83   REFINE.C  Region=Silicon Variable=Volume error.threshold=80 \
84             X.min=-100 X.max=100 Z.min=-100 Z.max=100 Y.min=0.0 Y.max=0.35
85
86   REFINE.C  Region=Silicon Variable=Volume error.threshold=30 \
87             X.min=-ld X.max=ld Z.min=-100 Z.max=100 Y.min=0.0 Y.max=0.05
88
89   REFINE.C  Region=Silicon Variable=Doping Measure=SignedLog error.threshold=0.7
90
91   METHOD    Type=Poisson
92   SOLVE
93
94   EXPORT    VTKFILE=inverter.vtk cgnsfile=inverter.cgns
```

In line 7, we instruct GENIUS to load mesh from files with names starting with *inverter.1*. We also specify the options to the TetGen mesh generation that are used during mesh refinements.

Lines 13-22 are provided in the skeleton input file, various regions in the model are

defined here, and are associated with their respective IDs in the mesh file. Similarly, surface labels are defined in line 25.

Some readers may have noticed that the gates of the NMOSFET and the PMOSFET are disconnected, while they should actually be joined. They are intentionally separated here, since the two parts of the polysilicon gate have very different workfunction, as specified in line 27-28. An abrupt change in workfunction leads to large local electric field, which requires unnecessarily dense meshes. It appears to us a better solution to leave a gap in-between, and connect the two parts later on.

The various doping profiles in lines 31-81 are provided in the skeleton, although the user certainly wants to tune the parameters in the y-direction according to the actual fabrication processes.

In lines 83-84, we first refine the surface region using the cell volume as the refinement criterium. In lines 86-87, we further refine the regions under the gate. Finally, in 89, we refine the junction regions using the gradient of doping concentration as the criterium. The resulting mesh for the inverter has about 48,000 nodes, and is shown in **Figure 2**, **p. 5**. A top view is show in **Figure 3**, **p. 6**, with all the contacts labelled. The doping profiles are shown in **Figure 4**, **p. 6** and **Figure 5**, **p. 7**.

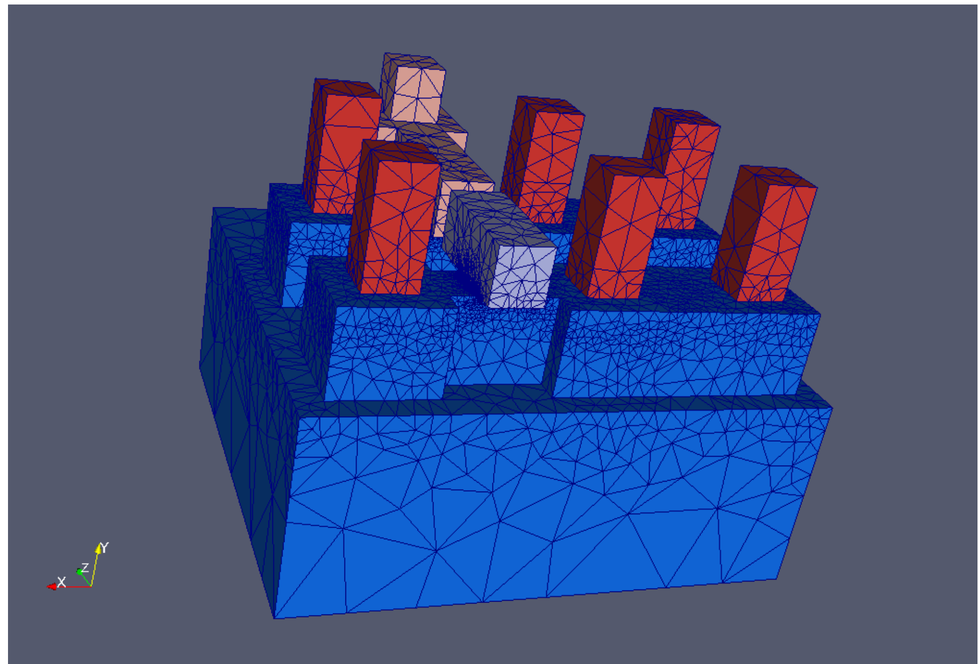


**Figure 2** The refined mesh of the CMOS inverter, with the oxide region stripped off.

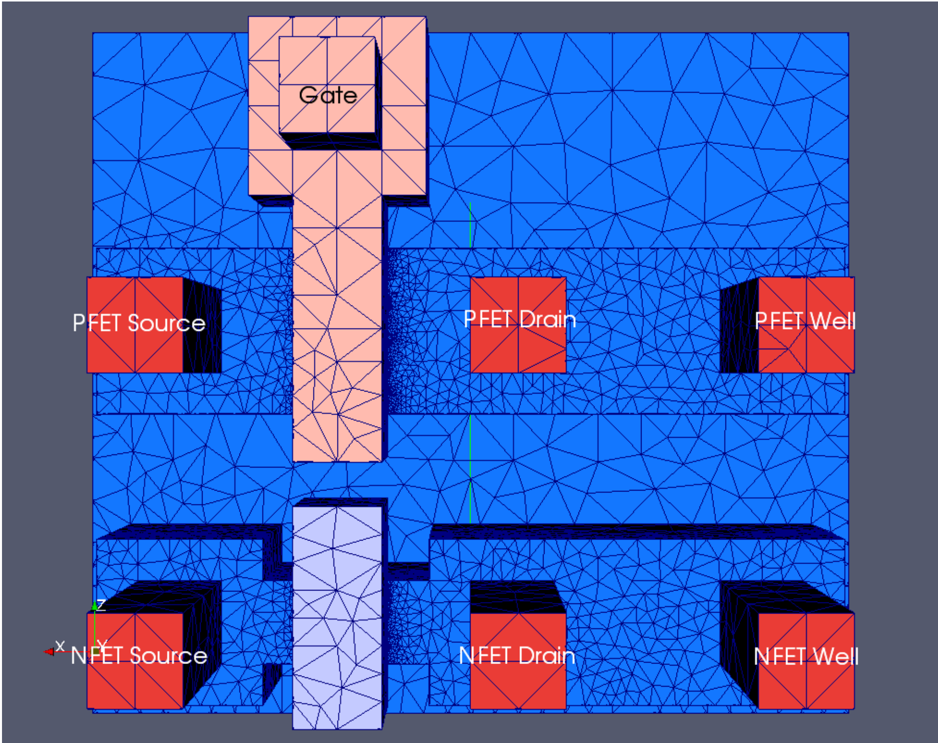


**Figure 3** Layout of the CMOS inverter.

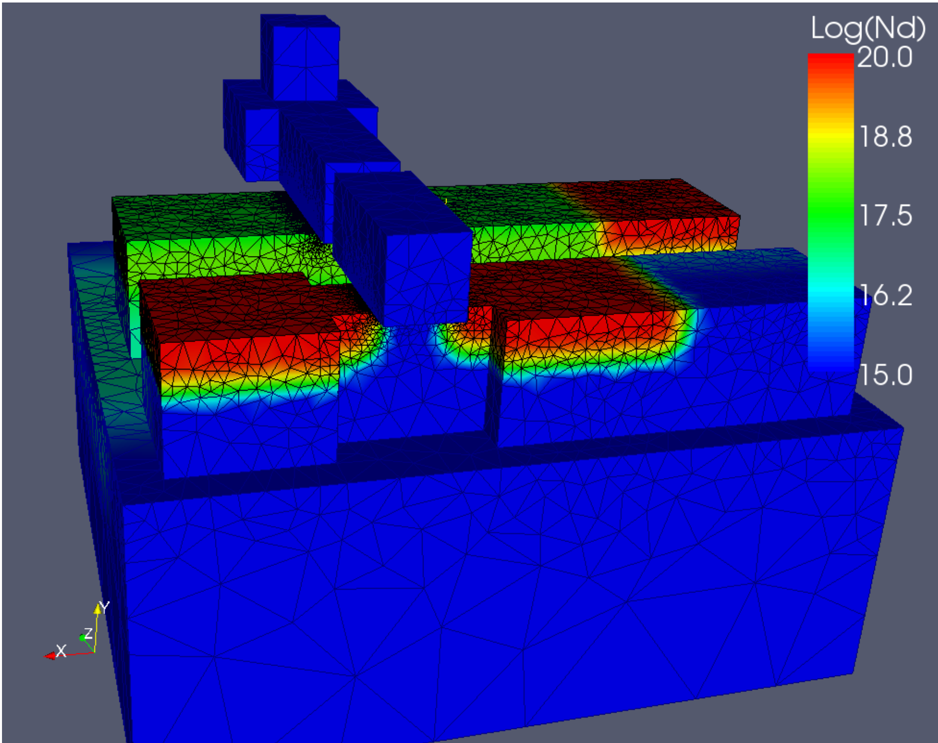


**Figure 4** Donor concentration in the inverter.

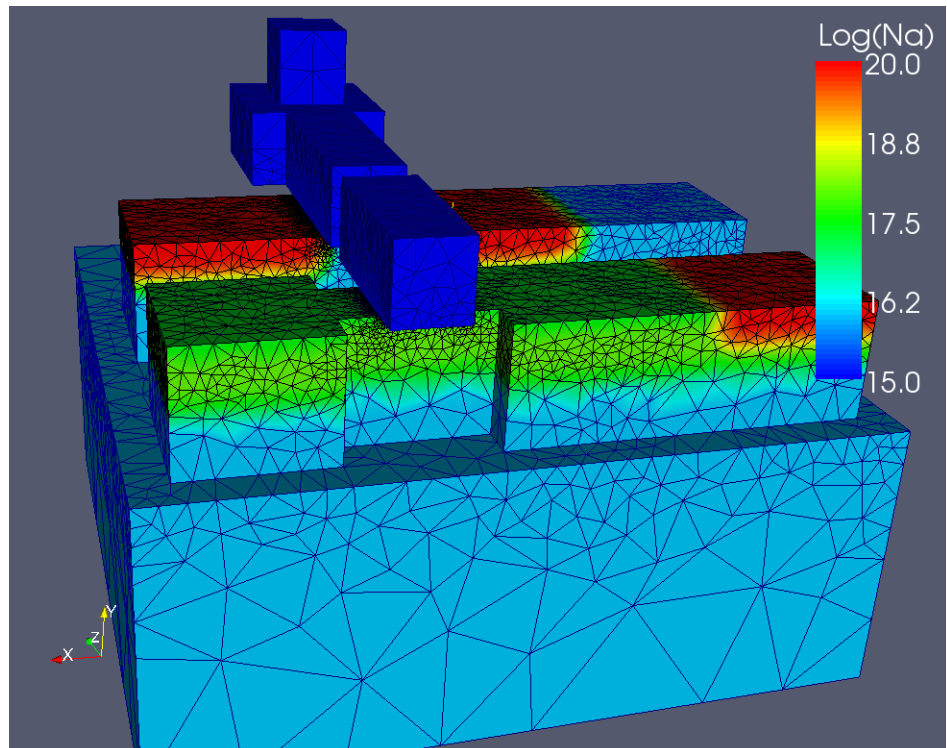


**Figure 5** Acceptor concentration in the inverter.

# Simulation of the Switching Characteristics

With the device structure generated, we can now proceed to simulate the switching curve of the inverter.

Input file to simulate the DC switching characteristics of the inverter.

```
1   #==============================================================================
2   # GENIUS Example. Do IV Scan at Vdrain=0.1V
3   #==============================================================================
4
5   GLOBAL    T=300 DopingScale=1e18
6
7   # voltage sources are needed here.
8   Vsource  Type = VDC    ID = VVDD    Tdelay=0   Vconst=1.8
9   Vsource  Type = VDC    ID = VGND    Tdelay=0   Vconst=0
10
11  # Load mesh
12  IMPORT    cgnsfile=inverter.cgns
13
14  BOUNDARY ID=Sub    Type=Ohmic Res=100
15
16  CONTACT  ID=NGate   Type=GateContact Workfunction=4.17 Res=0
17  CONTACT  ID=PGate   Type=GateContact Workfunction=5.20 Res=0
18  CONTACT  ID=NSource Type=Ohmic Res=10
19  CONTACT  ID=NDrain  Type=Ohmic Res=10
20  CONTACT  ID=PSource Type=Ohmic Res=10
21  CONTACT  ID=PDrain  Type=Ohmic Res=10
22  CONTACT  ID=NWell Type=Ohmic Res=10
23  CONTACT  ID=PWell Type=Ohmic Res=10
24
25  # Define the interconnects
26  INTERCONNECT ID=VIN  ConnectTo=NGate   ConnectTo=PGate   Res=0
27  INTERCONNECT ID=VDD  ConnectTo=PSource ConnectTo=PWell   Res=0
28  INTERCONNECT ID=VSS  ConnectTo=NSource ConnectTo=NWell   Res=0
29  INTERCONNECT ID=VOUT ConnectTo=PDrain  ConnectTo=NDrain  Res=0
30
31  # Attach voltage sources
32  ATTACH    Electrode=VDD Type=Voltage VApp=VVDD
33  ATTACH    Electrode=VIN Type=Voltage VApp=VGND
34  ATTACH    Electrode=VSS Type=Voltage VApp=VGND
35
36  # Solve the equilibrium state
37  Model     Region=Silicon H.Mob=false
```

```
38 METHOD   Type=DDML1 NS=Basic LS=MUMPS maxiteration=40 Damping=Potential
39 SOLVE    Type=STEADY
40
41 # Set physical models
42 PMI      Region=Silicon Type=Mobility Model=Lucent
43 Model    Region=Silicon H.Mob=true Mob.force=EQF
44 METHOD   Type=DDML1 NS=Basic LS=MUMPS maxiteration=40 Damping=Potential \
45          Toler.Relax=1e5
46
47 # Ramp up VDD
48 SOLVE    Type=DC  Vscan=VDD Vstart=0.0 Vstep=0.1 Vstop=1.8
49
50 # Scan input voltage
51 SOLVE    Type=DC  Vscan=VIN Vstart=0.0 Vstep=0.05 Vstop=1.8 out.prefix=gate_iv
52
53 EXPORT   VTKFILE=inverter_iv.vtk
```

The command `INTERCONNECT` is used in lines 26-29 to connect the electrodes of the two MOSFET to form the inverter circuit. The two parts of the gate are connected to the wire *VIN*. The two drain terminals are connected to the wire *VOUT*. The source of the NMOSFET and PMOSFET are tied to *VDD* and *VSS*, respectively. The user can specify the resistance between the wire and the device with the `CONTACT` command, and the resistance between the wire and the external voltage source in the `INTERCONNECT` command. Additionally, the wire can optionally have a shunt capacitance to ground and a series inductance to the external source.

We first solve the inverter in equilibrium state, where all terminals are grounded. We then ramp up the supply voltage at the wire *VDD*, from 0 to 1.8 V. Finally, the input voltage is scanned to obtain the switching characteristics. The simulated $V_{out}$ v.s. $V_{in}$ curve is plotted in **Figure 6**, **p. 10**, and the electrostatic potential in the inverter at $V_{in} = 1.8$ V is shown in **Figure 7**, **p. 10**.

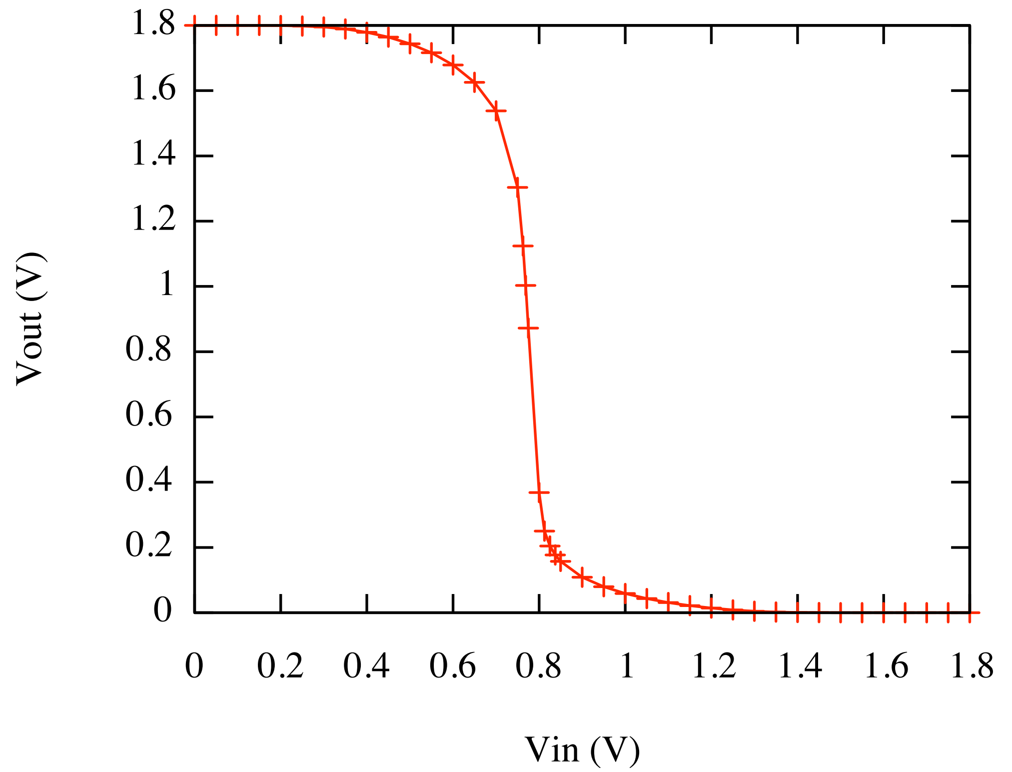


**Figure 6** Simulated switching characteristics of the inverter.

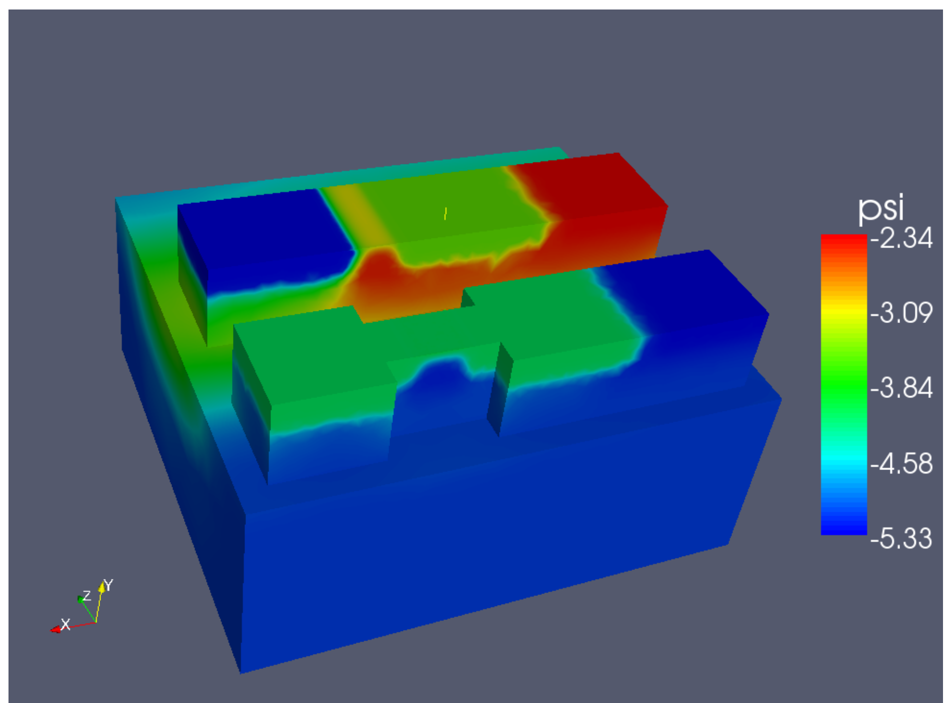


**Figure 7** Potenital profile in the inverter at $V_{in}$ = 1.8 V.

## Summary

The simulation of a 3D inverter circuit model is demonstrated in this chapter. The relatively large simulation can still be run in a laptop computer. However, it is certainly desirable to take advantage of modern parallel computers for much shorter simulation time. **Figure 8**, **p. 11** shows the run time of the inverter switching simulation on a cluster as a function of the number of processor cores used.

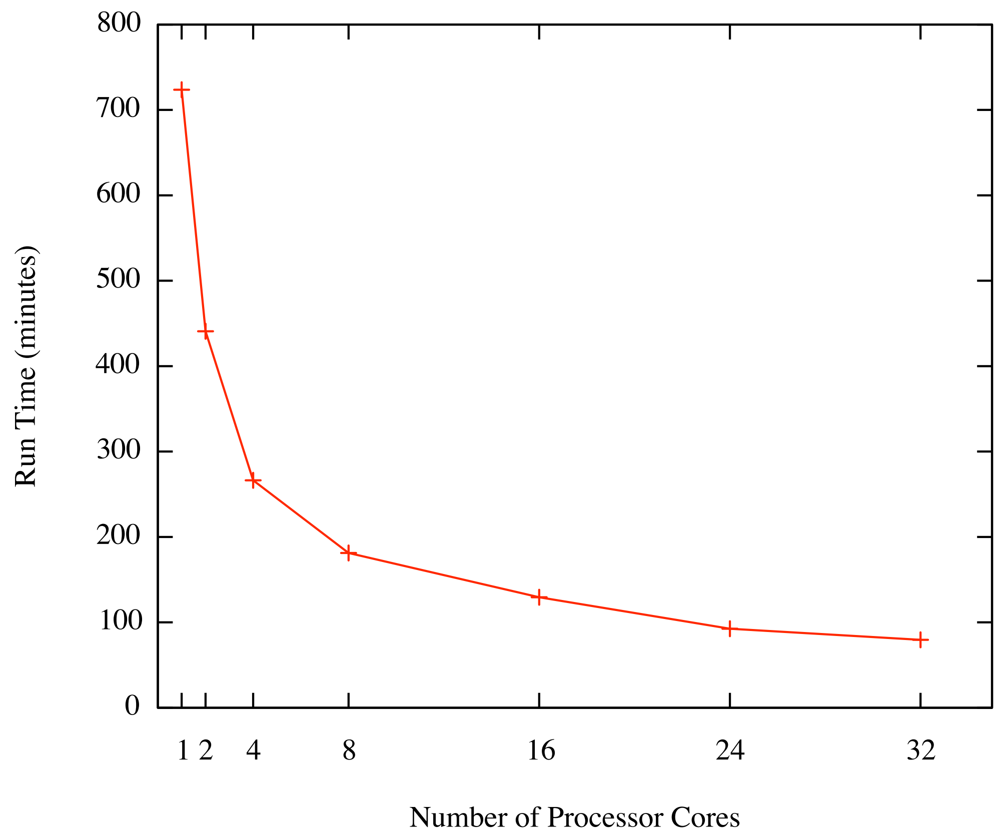


**Figure 8** Run time for inverter switching simulation.

In this test, the sweep of *VIN* from 0 to 1.8 V takes 724 minutes in serial simulation. With 32 cores, the simulation time is reduced to 79 minutes, showing speed up of nearly ten times. In **Figure 9**, **p. 12**, it is obvious that the speed-up from parallel computation scales very well as the number of processor cores increases, and further speed-up can be expected with additional processors.

The cluster computer used in this test has four nodes, and each node has two quad-core Xeon processors running at 2.66 GHz. The nodes are connected with Infiniband DDR interconnections. At the time of writing, the hardware cost of the cluster is approximately USD10,000.

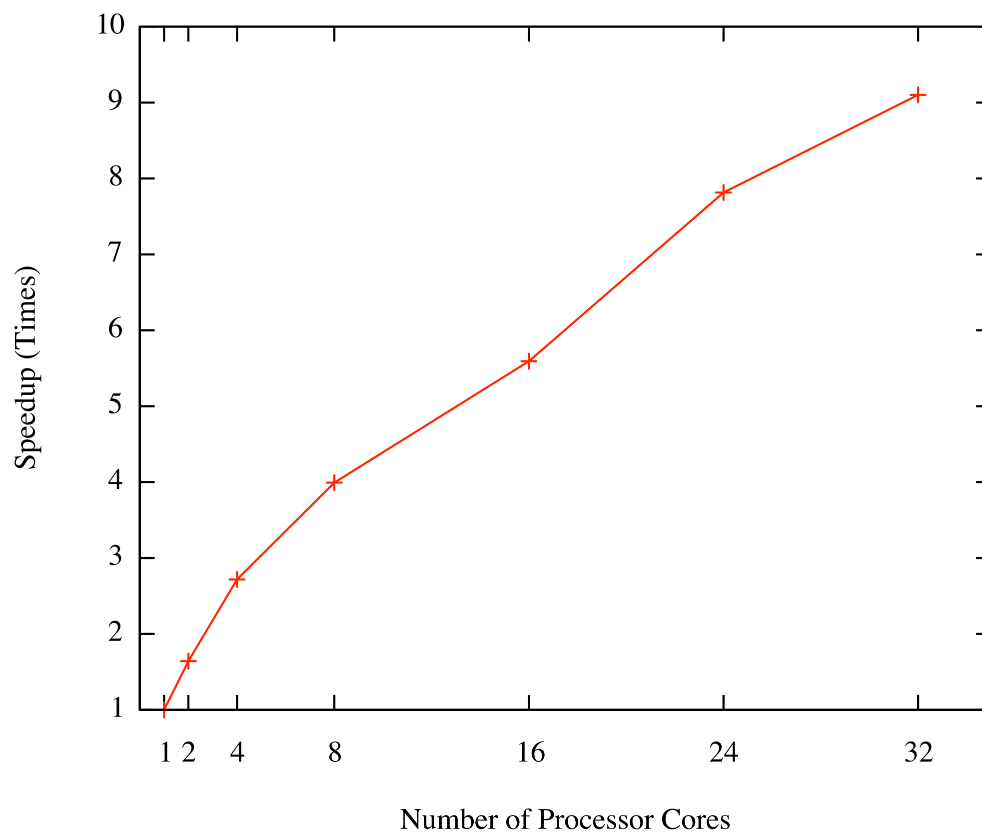


**Figure 9** Parallel speed-up.

The capability of simulating circuit cells with parallel computers allows users to analyze nanoscale circuits with GENIUS with reasonable throughput. It makes GENIUS the enabling tool for studying the interaction between fabrication processes and the circuit performance.